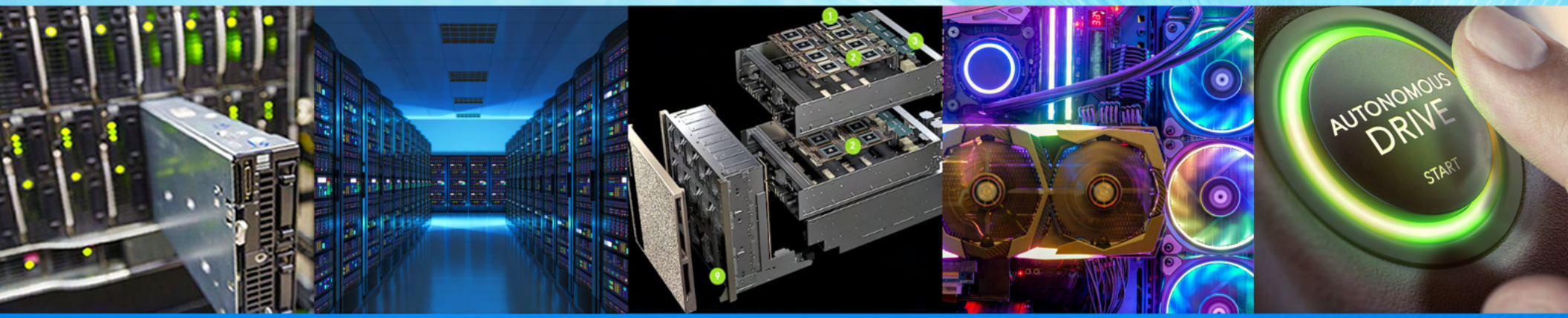
EFFICIENT POWER CONVERSION

48 V = GaN

eGaN® FETs and ICs for High Density Servers



AUTOMOTIVE MOBILE ROBOTICS SERVER SOLAR SPACE TELECOM

GaN-Based 48 V DC-DC

GaN technology is transforming 48 V

The advent of 5G and the explosion of data for hyperscalers, cloud-based data centers, and artificial intelligence demand more power in much smaller form factors.

Due to the significant improvements GaN offers in switching performance and size reduction, power supply designers are realizing that GaN FETs make higher power density and more efficient 48 V power supplies. These supplies are needed in high-density computing applications for cloud computing, artificial intelligence, machine learning, and multi-user gaming applications.

These advanced applications are putting higher load current demands on the power converters to support CPU, GPU, ASIC, and xPU, and silicon-based power conversion is not keeping pace.

GaN devices ***increase the efficiency, shrink the size, and reduce system cost*** for 48 V power conversion.

Benefits of migrating to 48 V

- **Easy delivery and distribution of higher power**
- **Solve challenges of current ecosystem**
  - -- Cabling and connectors
  - -- Distribution losses
  - -- Total cost of ownership
- **Build on industry proven 54 V or 48 V infrastructure**
- **Improve system efficiency**
  - -- 1/16 of front-end distribution losses
- **4x power transmission and 1/4 of the current**

48 V markets demanding eGaN technology

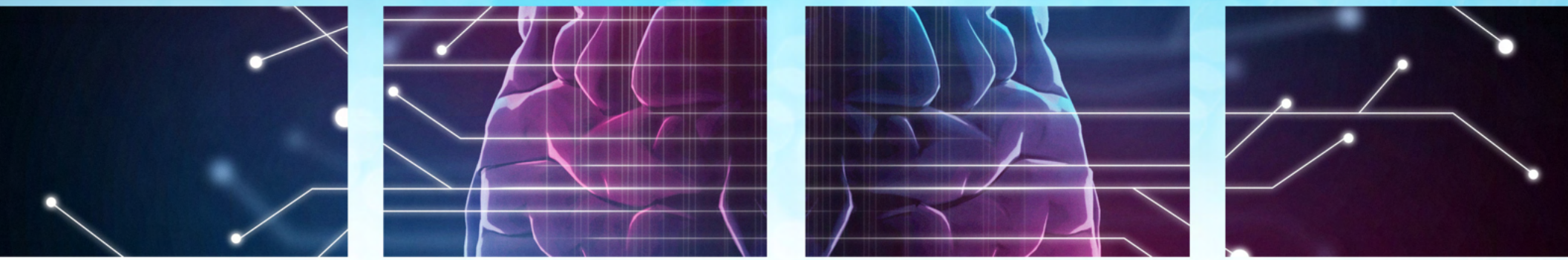
- **Artificial intelligence**
- **High density data centers**
- **Gaming**
- **12 V to 48 V to add 48 V AI legacy to 12 V PDN systems**
- **48 V to 12 V to power legacy 12 V circuity in 48 V servers**

eGaN-based 48 V – 12 V and 48 V – 5 V converter

Newer, high-power systems, like artificial intelligence (AI) systems powering high current GPU/xPU, and high power HPC/supercomputers are already adopting 48 V input.

The traditional approach consists of a two-stage conversion; from 48 V to lower intermediate voltage followed by a secondary stage using digital multiphase controller and power stages to power CPU/GPU/ASIC/xPU.

Existing systems require an additional bidirectional block to enable the 48 V migration. A 12 V to 48 V conversion to add 48 V AI to legacy 12 V PCN systems, or a 48 V to 12 V conversion to power legacy 12 V circuitry in 48 V servers.



GaN-based 48 V to 12 V buck converter

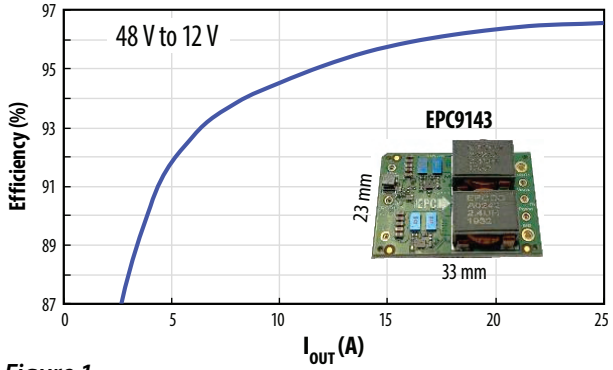


Figure 1.

Figure 1 presents an example of a GaN-based 48 V to 12 V buck design.

The EPC9143 uses the 100 V eGaN FET, EPC2053, to achieve 96.6% efficiency up to 25 A (300 W) in a very small 1/16th brick form factor. This represents a power density > 610 W/in³.

With an input voltage range of 7.5 V – 64 V and out put voltage range of 5 V – 20 V, this same design can be configured for a boost 12 V to 48 V, or a bi-directional 12 V – 48 V conversion.

GaN-based LLC for AI and 48 V front end modules

For high-density server applications, record power density and efficiency can be realized with simple topologies such as a DC-DC converter using an LLC topology. eGaN FETs are well suited for LLC converters due to their combined low gate charge (Q_G) with 5 V gate operation that yields very low gate power consumption, ultra-low on-resistance, and low output capacitance charge (Q_{OSS}).

In **figure 2,** a power density of about 1700 W/in³ (104 W/cm³) is achieved with an overall efficiency above 98% using a GaN-based LLC solution.

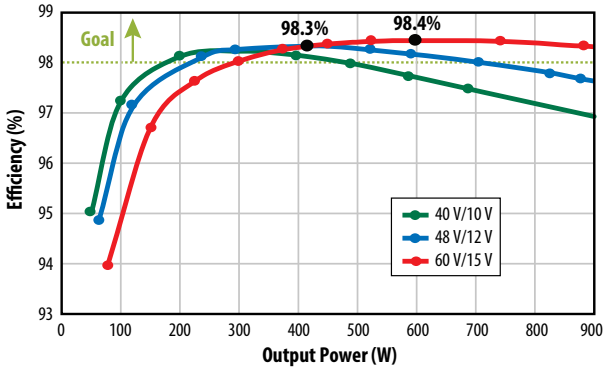
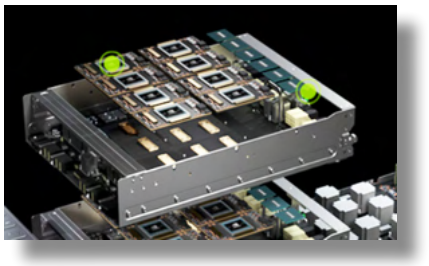
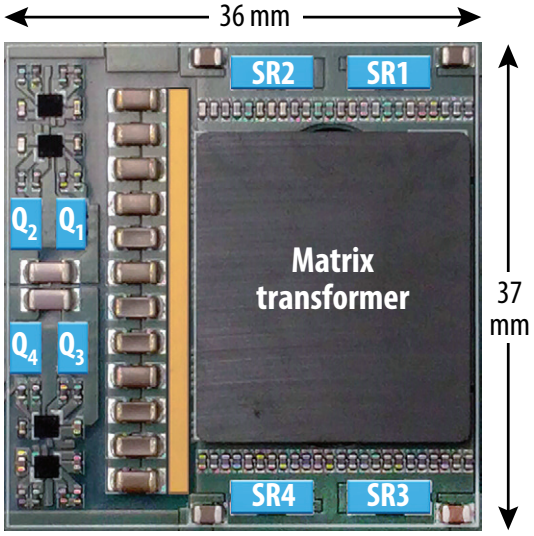
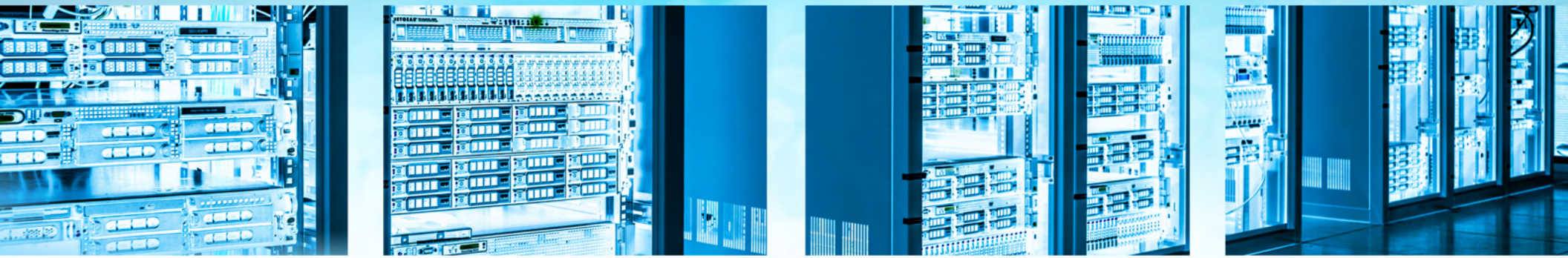


Figure 2.







There is also increasing interest in a power architecture that converts 48 V to 5 V and then uses integrated BCDMO for the point-of-load solution. There are several advantages to this approach.

Advantages of 48 V to 5 V LLC front end:

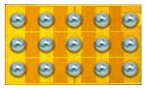
- **Allows > 1 MHz 5 V multiphase secondary stage with inductor height ~ of approximately 2 mm.**
- **Reduces secondary stage size**
- **Improves overall efficiency by fitting point-of-load (POL) solution closer to xPU/ASIC/GPU and below the heat sink.**
- **Can be plugged in vertically for extra space savings**

Benchmark 100 V eGaN® FET vs. best in class 80 V MOSFET

As shown in **figure 3**, which is a comparison of the best-in-class 80 V silicon device to the latest generation 100 V eGaN FET the improvements are astounding.

EPC eGaN FETs are significantly smaller and more efficient than the MOSFET benchmark. Additionally, eGaN FETs allow higher switching frequency for reduced solution.

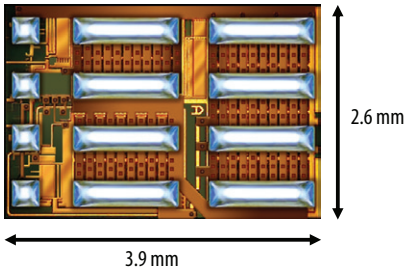
80 V MOSFET Benchmark 3.3 mm x 3.3 mm

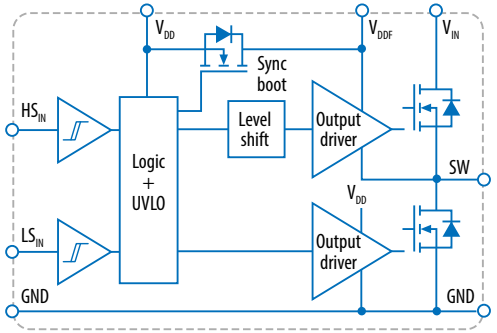


EPC2045 100 V eGaN FET Benchmark 1.5 mm x 2.5 mm

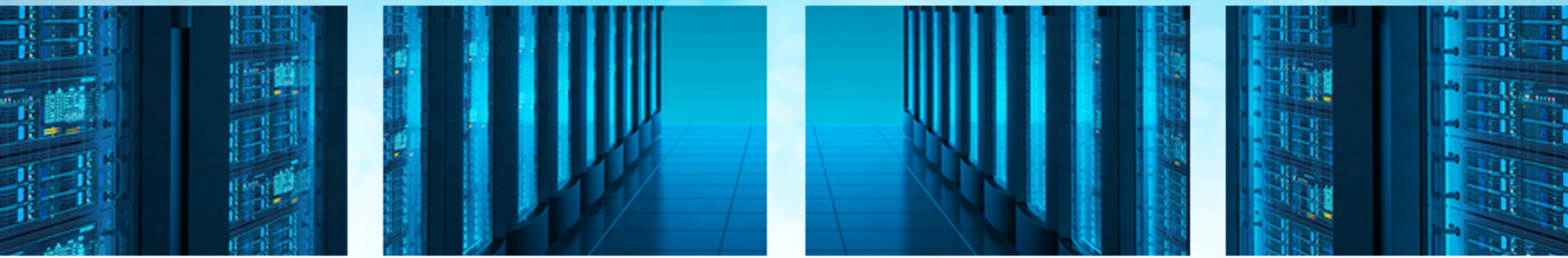
	MOSFET Benchmark 5 V V_{GS}	EPC2045 5 V V_{GS}	EPC GaN FET Improvement
$R_{DS(on)}$ typ	7.2 mΩ	5.6 mΩ	22%
$R_{DS(on)}$ max	9.2 mΩ	7 mΩ	24%
Q_G typ	15 nC	5.9 nC	60%
Q_{GD} typ	5 nC at 40 V_{DS}	0.8 nC at 50 V_{DS}	84%
Q_{OSS} typ	29 nC at 40 V_{DS}	25 nC at 50 V_{DS}	14%
Q_{RR} typ	29 nC at 40 V_R V	0 nC	Inf.
R_G typ	1.3 Ω	0.6 Ω	54%
Charge ratio	1.6	0.6	63%
Device size	10.9 mm²	3.75 mm²	66%

Figure 3.





Integration in GaN makes your system even *faster and smaller!*



Best 100 V FETs in the world

The latest generation **(figure 4)** of 100 V GaN devices offer the lowest $R_{DS(on)}$ in the smallest size to increase the efficiency, shrink the size, and reduce system cost for 48 V power conversion. In all the topologies with 48 V input, the highest efficiency comes with using GaN devices.

EPC custom integration

EPC also offers custom integration to allow users to form-fit their solution. GaN is a lateral device so it is relatively easy to integrate. To discuss requirements for a custom GaN solution, contact us at info@epc-co.com

Get started fast – design tools

To aid designers with fast prototyping and evaluation low-cost, easy-to-use demo boards are ideal for evaluating the features and capabilities of EPC eGaN FETs and ICs. Quick Start Guides, schematics, bills of materials, and Gerber Files are available for all boards for quick reference and use. For a full list of available demo boards visit epc-co.com/epc/Products/DemoBoards.aspx

Scan for more information:

100 V Device Portfolio	1.3 mm x 0.85 mm	1.5 mm x 1.5 mm	1.5 mm x 2.5 mm	2 mm x 3.5 mm
Parameter	**EPC2051 (at 5 V V_{GS})**	**EPC2052 (at 5 V V_{GS})**	**EPC2045 (at 5 V V_{GS})**	**EPC2053 (at 5 V V_{GS})**
$R_{DS(on)}$ typ	20 mΩ	10 mΩ	5.6 mΩ	3.2 mΩ
$R_{DS(on)}$ max	25 mΩ	12.5 mΩ	7 mΩ	4 mΩ
Q_G typ	1.7 nC	3.7 nC	5.9 nC	12 nC
Q_{GD} typ	0.3 nC at 50 V_{DS}	0.5 nC at 50 V_{DS}	0.8 nC at 50 V_{DS}	1.5 nC at 50 V_{DS}
Q_{OSS} typ	7.3 nC at 50 V_{DS}	13 nC at 50 V_{DS}	25 nC at 50 V_{DS}	43 nC at 50 V_{DS}
Q_{RR} typ	0 nC	0 nC	0 nC	0 nC
R_G typ	0.8 Ω	0.7 Ω	0.6 Ω	0.6 Ω
Charge ratio	0.6	0.5	0.6	0.5
Device size	1.1 mm^2	2.25 mm^2	3.75 mm^2	7 mm^2

Figure 4. ***Lowest $R_{DS(on)}$ in smallest size; ideal for integration on substrate or leadframe***